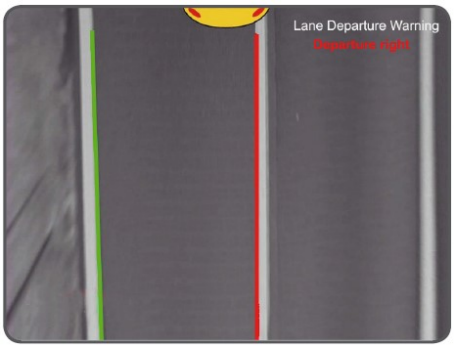
LMD Lane Marking Detector

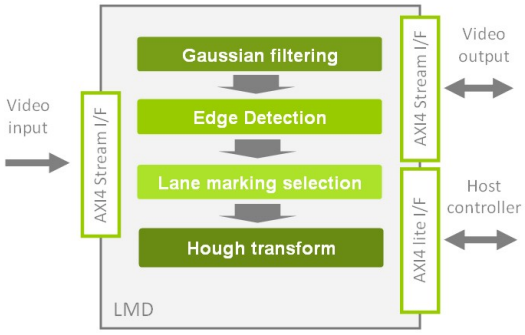
GENERAL DESCRIPTION

LMD Lane Marking Detector IP core is designed to detect roadway lane markings. It operates on a stream from a rear view camera warped in the bird eye view space. The output of the core is the set of extracted straight lines corresponding to lane markings. The algorithm parameters are fully programmable via software.
The core uses a model fitting algorithm based on Hough Transform and is robust to noise, shadows and light changes.
LMD is the fundamental building block for a FPGA-based Rear Looking Lane Departure Warning System.



CORE FEATURES	
Xilinx® family target	Zynq®-7000 AP SoC
Design file format	Encrypted VHDL (Vivado Core)
Register interface	ARM AMBA AXI4 compliant
Input interface	AXI4 Stream slave
Input format	RGB/YUV Image size up to 800x600
Output interface	AXI4 Stream master (optional) Output video shows the results of the processing stages for development and demonstration purpose.
Input data rate	> 180 Mpixel/sec
Frame rate	> 300 fps (800x600 resolution)
Additional items	SW drivers, API and post processing library available

ARCHITECTURE



APPLICATIONS

- Lane departure warning systems
- Autonomous navigation

IMPLEMENTATION STATISTICS FOR XILINX FPGAS

Family (Device)	Fmax (Mhz)	FFs	LUTs	BRAM18	DSP48	Design Tools
Zynq-7000 (XC7Z020-2)	200	4,204	3,158	14	15	Vivado 2016.4

eVS CONTACTS:

eVS embedded Vision Systems Srl
c/o Computer Science Park
Strada Le Grazie, 15, 37134 - Verona, Italy
tel/fax: +39 045 8027027

web: www.embeddedvisionsystems.it
email: info@evsys.it
To request a quotation:
email: sales@evsys.it

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